Ayal Zaks

CONTACT INFORMATION

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RESEARCH INTERESTS

Compiler Optimizations; Parallel Architectures, including Thread, Data and Instruction Level Parallelism; Compiler Analysis and Transformations targeting architectures to exploit such parallelism.

PROFESSIONAL EXPERIENCE

Intel

Leader, Software Engineer **2012 – now**
Working on Intel LLVM-based compiler optimizations for Intel platforms.
Member of the LLVM Open-Source Developers Community.

Princeton University

On HiPEAC Sabbatical **7.2011 – 10.2011**
Collaborating with Liberty computer architecture research group led by Prof. David August.

IBM Haifa Research Lab **1997 – 2011**

Manager of Compiler Technologies group **2004 – 2011**
1st-line manager of up to a dozen group members, involved in R&D of advanced compilation techniques and compiler optimizations. Focused on exploitation of Power architectures. Contributing optimizations to GCC and IBM compilers. Led IBM's participation in European FP6 project ACOTES, FP7 project ERA, and participant in FP6 project MilePost.

GCC Compiler Team Leader **2002 – 2004**
Leading a compiler research and development team contributing to GCC's performance on PowerPC platforms. Involved in optimizations for PowerPC970/Apple G5, including auto-vectorization for multi-media extensions (such as AltiVec) and modulo-scheduling.

DSP Compiler Team Leader **2001 – 2002**
Leading a DSP compiler R&D team (www.research.ibm.com/elite/Compiler/compiler.html).

IBM T.J.Watson Research Center

On international assignment **2000 – 2001**
Working on an optimizing compiler for a DSP.

IBM Haifa Research Lab

Compiler Team Member **1997 – 2000**
Engaged in performance improvement of compilers, static memory disambiguation, loop unrolling, instruction scheduling, static branch prediction, global analysis of Java for call de-virtualization.

IET Intelligent Electronics (renamed ClickSoftware Technologies), Tel-Aviv

Software Developer **1992 – 1996**
Experienced in developing (1) graph algorithms and computational geometry, (2) probabilistic models for solving real-world situations, (3) SW infrastructure of a Blackboard Framework.

Education

Tel Aviv University, Tel Aviv, Israel. *Department of Mathematics/Operations Research*
Ph.D., 2002

- Dissertation Topic: "Coloring Problems in Combinatorics"
- Advisor: Prof. Noga Alon

M.Sc., with honors (final grade 93), 1997

- Dissertation on: "Restricted Vertex-Colorings of Graphs in Frequency Assignment Problems"
- Advisor: Prof. Noga Alon

B.Sc., with honors, 1994

Honors and Awards

IBM Outstanding Technical Achievement Award, 2008

IBM Research Division Group Award, 2004

On the list of distinguished Ph.D. students, School of Mathematics, 1997

Dean's list of distinguished B.Sc. students, Tel Aviv University, 1992 and 1993.

Academic Experience

Technion, Israel Institute of Technology, Haifa, Israel

Adjunct Lecturer **2009 – present**
Formal Languages and Compilation 46266, dept. of Electrical Engineering **2008 – present**
Theory of Compilation 236360 course in the Department of Computer Science **2006**

ACACES Summer School, L'Aquila and Fiuggi, Italy **July 2005, 2014**

Taught a course on "Heterogeneous Compilation using OpenCL" at the 10th International Summer School and a course on "Optimizations in GCC" at the 1st International Summer School on *Advanced Computer Architecture and Compilation for Embedded Systems*.

Haifa University, Haifa, Israel **2004**

Taught the *Theory of Compilation* course in the Department of Computer Science.

Chair of: PACT'16 (general), CC'16 (general), HiPEAC'14 (program), CGO'11 (workshops).
On program committee of: CGO'18, CGO'17, CC'15, IPDPS15, ICS'14, CC'14, CGO'13, PACT'13, IPDPS'13, VMIL'13, COSMIC'13, CGO'11, HiPEAC'11, GROW'11, WRC'11, ICS'10, GROW'10, WRC'10, MEDEA'09, SMART'07, PAC'2, DATE'05, CTCES'04. On the ERC of PACT'17, PLDI'17. Distinguished Reviewer for ACM TACO 2014, 2015, 2016. Reviewer of HiPEAC'12, PPoPP'12.

Co-supervised Technion/CS M.Sc. student (Liza Fireman, 2006).
Co-supervising Technion/EE Ph.D. student (Nathaniel Azuelos, 2010–).
Co-supervising Haifa University/CS M.Sc. student (Gil Rapaport, 2011–2014).
Co-supervised a Harvey Mudd College Clinic project with the Technion (2012/13).

On the Ph.D. committee of:

- Sean Rul, *Profile-Driven Discovery of Parallelism for Multi-Core Processors*, Ghent U., 2010.
- Paul Carpenter, *Running Stream-like Programs on Heter. Multi-Core Systems*, UPC, 2011.
- Konrad Trifunovic, *Effcient search-based strategies for polyhedral compilation: Algorithms and experience in a production compiler*, Universit Paris-Sud 11, 2011.
- Victor Lomüller, *Multi-Time Code Generation and Multi-Objective Code Optimization*, U. of Grenoble, 2014.
- Diego Luis Caballero De Gea, *SIMD@OpenMP: A Programming Model Approach to Leverage SIMD Features*, UPC, 2015.
- Andrew Anderson, *Vectorization for Accelerated Gather/Scatter and Multibyte Data Formats*, Trinity College Dublin, 2016.
- Diogo Sampaio, *Profile Guided Hybrid Compilation*, INRIA, Grenoble, 2016.

On the M.Sc. committee of:
Yuval Shimron, *Smaller Footprint for Java Collections*, Technion, 2011;
Moshe Yuda, *Source Level Merging of Independent Programs*, Haifa University, 2007).

Occasionally refereed papers of Discrete Mathematics, Discrete Applied Mathematics, Journal of Graph Theory, and Discrete Optimization.

Member of HiPEAC. Hosted eight 3-month summer HiPEAC Ph.D. student internships.

Member of ACM.

PUBLICATIONS (CONFERENCES)

1. Nick P. Johnson, Taewook Oh, Ayal Zaks and David I. August, *Fast condensation of the program dependence graph*, ACM SIGPLAN 2013 Conference on Programming Language Design and Implementation (PLDI), June 16–22, 2013, Seattle, WA, USA. pp. 39–50.
2. Per Larsen, Razya Ladelsky, Jacob Lidman, Sally A. McKee, Sven Karlsson and Ayal Zaks, *Parallelizing more Loops with Compiler Guided Refactoring*, 41st International Conference on Parallel Processing (ICPP), Sept 10–13, 2012, Pittsburgh, PA, USA. pp. 410–419.
3. Arun Raman, Ayal Zaks, Jae W. Lee and David I. August, *Parcae: A System for Flexible Parallel Execution*, ACM SIGPLAN 2012 Conference on Programming Language Design and Implementation (PLDI), June 11–16, 2012, Beijing, China.
4. Nick P. Johnson, Hanjun Kim, Prakash Prabhu, Ayal Zaks and David I. August, *Speculative Separation for Privatization and Reductions*, ACM SIGPLAN 2012 Conference on Programming Language Design and Implementation (PLDI), June 11–16, 2012, Beijing, China.
5. Nathaniel Azuelos, Idit Keidar and Ayal Zaks, *Tolerant Value Speculation in Coarse-Grain Streaming Computations*, 25th IEEE International Parallel and Distributed Processing Symposium (IPDPS), May 16 – 20, 2011, Anchorage, Alaska.
6. Dorit Nuzman, Sergei Dyshel, Erven Rohou, Ira Rosen, Kevin Williams, David Yuste, Albert Cohen and Ayal Zaks, *Auto-Vectorize Once, Run Everywhere*, International Symposium on Code Generation and Optimization (CGO), April 2 – 6, 2011, Chamonix, France. pp. 151 – 160.
7. Erven Rohou, Kevin Williams, Albert Cohen, Sergei Dyshel, Dorit Nuzman, Ira Rosen, and Ayal Zaks, *Speculatively Vectorized Bytecode*, The 6th International Conference on High Performance and Embedded Architectures and Compilers (HiPEAC), January 24 – 26, 2011, Heraklion, Crete, Greece. pp. 35 – 44.
8. Mircea Namolaru, Grigori Fursin, Albert Cohen, Ari Freund and Ayal Zaks, *Practical Aggregation of Semantical Program Properties for Machine Learning Based Compilation*, International Conference on Compilers Architectures and Synthesis for Embedded Systems (CASES), October 24 – 29, 2010, Scottsdale, AZ, USA. pp. 197 – 206.
9. Alfred J. Park, Cheng-Hong Li, Ravi Nair, Nobuyuki Ohba, Uzi Shvadron, Ayal Zaks and Eugen Schenfeld, *Flow: A Stream Processing System Simulator*, 24th ACM/IEEE/SCSWorkshop on Principles of Advanced and Distributed Simulation (PADS), May 17 – 19, 2010, Atlanta, GA.
10. Olga Golovanevsky, Alon Dayan, Ayal Zaks and David Edelsohn, *Trace-Based Data Layout Optimizations for Multi-Core Processors*, The 5th International Conference on High Performance and Embedded Architectures and Compilers (HiPEAC) (Best Paper Award), January 25 – 27, 2010, Pisa, Italy. pp. 81 – 95.
11. Konrad Trifunovic, Dorit Nuzman, Albert Cohen, Ayal Zaks and Ira Rosen, *Polyhedral-Model Guided Loop-Nest Auto-Vectorization*, The Eighteenth International Conference on Parallel Architectures and Compilation Techniques (PACT), September 12 – 16, 2009, Raleigh, NC. pp. 327 – 337.

12. Ira Rosen, Ben Elliston, Revital Eres, Alan Modra, Dorit Nuzman, Ulrich Weigand, Ayal Zaks, and David Edelsohn, *Compiling Effectively for Cell B.E. with GCC*, 14th Workshop on Compilers for Parallel Computing (CPC), January 7 – 9, 2009, Zurich, Switzerland.
13. Dorit Nuzman and Ayal Zaks, *Outer-Loop Vectorization - Revisited for Short SIMD Architectures*, The Seventeenth International Conference on Parallel Architectures and Compilation Techniques (PACT), October 25 – 29, 2008, Toronto, Canada. pp. 2 – 11.
14. Dorit Nuzman, Mircea Namolaru, Ayal Zaks, and Jeff H. Derby, *Compiling for an Indirect Vector Register Architecture*, ACM International Conference on Computing Frontiers 2008, May 5–7, Ischia, Italy. pp. 199–208.
15. Liza Fireman, Erez Petrank, and Ayal Zaks, *New Algorithms for SIMD Alignment*, 16th International Conference on Compiler Construction (CC), March 26–30, 2007, Braga, Portugal. pp. 1–15.
16. Dorit Nuzman, Ira Rosen, and Ayal Zaks, *Auto-Vectorization of Interleaved Data for SIMD*, ACM SIGPLAN 2006 Conference on Programming Language Design and Implementation (PLDI), June 11–14, 2006, Ottawa, Canada. pp. 132–143.
17. Dorit Naishlos, Shay Ben-David, Marina Biberstein and Ayal Zaks, *Vectorizing for SIMdD DSP Architecture* , International Conference on Compilers Architectures and Synthesis for Embedded Systems (CASES), October 30–November 1, 2003, San Jose, California, pp. 2–11. (Presented at a research seminar, IBM T.J. Watson Research Center, Yorktown Heights, NY, on Feb 3, 2003).
18. Ayal Zaks, Vitaly Feldman and Nava Aizikowitz. *Sealed Calls in Java Packages*, ACM Conference on Object-Oriented Programming, Systems, Languages, and Applications (OOPSLA), October 15–19, 2000, Minneapolis, MN, pp. 83–92.
19. Noga Alon and Ayal Zaks, *Progressions in Sequences of Nearly Consecutive Integers*, Journal of Combinatorial Theory (Series A), Vol. 84, No. 1, October 1998, pp. 99–109. (Presented at the 9th SIAM Conference on Discrete Mathematics, Toronto, July 12–15, 1998).
20. Noga Alon and Ayal Zaks, *T-choosability in graphs* , Discrete Applied Mathematics 28 (1998) pp. 1–13. (Presented at the International Colloquium on Combinatorics and Graph Theory, Balatonlelle, Hungary, July 1996, and at the Annual Israeli Mathematical Union meeting, Jerusalem, 1998).
21. Michael Naaman and Ayal Zaks, *Fractal Blackboard Framework* , 8th Israeli Conference on Computer Systems and Software Engineering (ICCSSE), June 18–19, 1997, Herzliya, Israel, pp. 23–29.

Publications (Journals and Book Chapter)

1. Alfred J. Park, Cheng-Hong Li, Ravi Nair, Nobuyuki Ohba, Uzi Shvadron, Ayal Zaks and Eugen Schenfeld, *Towards Flexible Exascale Stream Processing System Simulation*, SIMULATION Journal, Special Issue on the "Principles of Advanced and Distributed Simulation", Volume 88 Issue 7, July 2012, Pages 832-851
2. Harm Munk, Eduard Ayguade, Cedric Bastoul, Paul Carpenter, Zbigniew Chamski, Albert Cohen, Marco Cornero, Marc Duranton, Mohammed Fellahi, Roger Ferrer, Razya Ladelsky, Menno Lindwer, Xavier Martorell, Cupertino Miranda, Dorit Nuzman, Andrea Ornstein, Antoniu Pop, Sebastian Pop, Louis-Noel Pouchet, Alex Ramirez, David Rodenas, Erven Rohou, Ira Rosen, Uzi Shvadron, Konrad Trifunovic, Ayal Zaks, *ACOTES Project: Advanced Compiler Technologies for Embedded Streaming*, International J. of Parallel Processing (IJPP), Volume 39, Issue 3, June 2011 (Special Issue on European HiPEAC NoE member's projects), pp. 397 – 450.
3. Grigori Fursin, Zbigniew Chamski, Cupertino Miranda, Olivier Temam, Mircea Namolaru, Elad Yom-Tov, Ayal Zaks, Bilha Mendelson, Phil Barnard, Elton Ashton, Eric Courtois, Francois Bodin, Edwin Bonilla, John Thomson, Hugh Leather, Chris Williams, Michael O'Boyle, *Milepost GCC: A machine learning enabled self-tuning compiler*, International J. of Parallel

Processing (IJPP), Volume 39, Issue 3, June 2011 (Special Issue on European HiPEAC NoE member's projects), pp. 296 – 327.

4. Stephan Wong, Luigi Carro, Mateus Rutzig, Debora Motta Matos, Roberto Giorgi, Nikola Puzovic, Stefanos Kaxiras, Marcelo Cintra, Giuseppe Desoli, Paolo Gai, Sally A. Mckee, and Ayal Zaks, ERA Embedded Reconfigurable Architectures, (Chapter 10 in) Reconfigurable Computing: From FPGAs to Hardware/Software Codesign, Cardoso, João M. P. and Hübner, Michael (Eds.), 1st Edition., 2011, pp. 239 – 250.
5. Olga Golovanevsky, Alon Dayan, Ayal Zaks and David Edelsohn, *Architecture-Aware Data Layout Optimizations for Multi-Core Processors*, Transactions on High Performance Embedded Architectures and Compilers (HiPEAC), Volume 5, Issue 1, 2010, pp. 81 – 95.
6. Baruch Schieber, Danny Geist and Ayal Zaks, *Computing the minimum DNF representation of Boolean functions defined by intervals*, Discrete Applied Mathematics, Vol. 149, Issue 1-3, August 2005, pp. 154–173.
7. David Edelsohn et al., *Contributions to the GNU Compiler Collection GCC*, IBM Systems Journal issue on Open Source, Volume 44, Number 2, May 2005, pp. 259–278.
8. Jaime H. Moreno et al., *An innovative low-power high-performance programmable signal processor for digital communications*, IBM Journal of Research and Development, Vol. 47, No. 2/3, March/May 2003, pp. 299–326.
9. Noga Alon and Ayal Zaks, *Algorithmic Aspects of Acyclic Edge Colorings*, Algorithmica 32 (2002), pp. 611–614.
10. Noga Alon, Benny Sudakov and Ayal Zaks, *Acyclic edge-coloring of graphs*, Journal of Graph Theory, Vol. 37, Issue 3, (2001), pp. 157–167. (Presented at a Workshop on Theoretic Computer Science, IBM T.J. Watson Research Center, Yorktown Heights, NY, 1999).

PUBLICATIONS (WORKSHOPS, NON-REFEREED)

1. Gil Rapaport and Ayal Zaks, *Introducing VPlan to the Loop Vectorizer*, EuroLLVM Developers' Meeting, March 27–28, 2017, Saarbrüken, Germany.
2. Xinmin Tian, Hideki Saito, Ernesto Su, Abhinav Gaba, Matt Masten, Eric Garcia and Ayal Zaks, *LLVM Framework and IR Extensions for Parallelization, SIMD Vectorization and Offloading.* Third International Workshop on the LLVM Compiler Infrastructure in HPC, November 14, 2016, Salt Lake City, Utah. Colocated with the International Conference for High Performance Computing, Networking, Storage and Analysis (SC16).
3. Gil Rapaport, Ayal Zaks and Yosi Ben Asher, *C Higher Order Vector Semantics using Whole Function Vectorization*, Workshop on Programming Models, Languages and Compilers for Manycore and Heterogeneous Architectures (PLC), May 25th, 2015, Hyderabad, INDIA. Colocated with the 29th IEEE International Parallel & Distributed Processing Symposium (IPDPS 2015).
4. James Cownie, Simon McIntosh-Smith, Arik Narkis and Ayal Zaks, *Leverage Your OpenCL™ Investment on Intel® Architecture*, Intels Parallel Universe Magazine, Issue 18, June 2014.
5. Shahar Timnat, Ohad Shacham and Ayal Zaks, *Predicate Vectors If You Must*, Workshop on Programming Models for SIMD/Vector Processing, February 16, 2014, colocated with the 19th ACM SIGPLAN Symposium on Principles and Practice of Parallel Programming (PPoPP), Orlando, Florida, USA.
6. Alexander Heinecke, Dirk Pflüger, Dmitry Budnikov, Michael Klemm, Arik Narkis, Maxim Shevtsov and Ayal Zaks, *Demonstrating Performance Portability of A Custom OpenCL Data Mining Application to the Intel®Xeon Phi™Coprocessor*, International Workshop on OpenCL (IWOCL), May 12-13, 2013, Atlanta, GA, USA.
7. Alon Mishne and Ayal Zaks, poster on *LLVM IR editor plugin for Eclipse*, 2013 European LLVM Conference, April 29-30, 2013, Paris, France.

8. Nathaniel Azuelos, Yoav Etsion, Idit Keidar, Ayal Zaks, and Eduard Ayguadé, *Introducing Speculative Optimizations in Task Dataflow with Language Extensions and Runtime Support*, Workshop on Data-Flow Execution Models for Extreme Scale Computing (DFM), September 23, 2012, Minneapolis, USA.
9. Nicklas Bo Jensen, Per Larsen, Razya Ladelsky, Ayal Zaks and Sven Karlsson, *Guiding Programmers to Higher Memory Performance*, Fifth Workshop on Programmability Issues for Heterogeneous Multicores (MultiProg), January 23, 2012, Paris, France.
10. Per Larsen, Razya Ladelsky, Sven Karlsson and Ayal Zaks, *Compiler Driven Code Comments and Refactoring*, Third Swedish Workshop on Multi-core Computing (MCC), November 18 – 19, 2010, Göteborg, Sweden. Extended version accepted at the Fourth Workshop on Programmability Issues for Heterogeneous Multicores (MultiProg), January 23, 2011, Heraklion, Crete, Greece.
11. Nikola Puzović, Sally A. McKee, Revital Eres, Ayal Zaks, Paolo Gai, Stephan Wong and Roberto Giorgi, poster on *A Multi-Pronged Approach to Benchmark Characterization*, IEEE International Conference on Cluster Computing (Clusters), September 20 – 24, 2010, Heraklion, Crete, Greece.
12. Grigori Fursin et al., *Enabling dynamic selection of good optimization passes in MILEPOST GCC*, GCC Developers' Summit 2008, June 17–19, Ottawa, Canada. pp. 7–20.
13. Olga Golovanevsky and Ayal Zaks, *Struct-reorg: current status and future perspectives*, GCC Developers' Summit 2007, July 18–20, Ottawa, Canada. pp. 47–56.
14. Ira Rosen, Dorit Nuzman and Ayal Zaks, *Loop-based SLP*, GCC Developers' Summit 2007, July 18–20, Ottawa, Canada. pp. 131–142.
15. Dorit Nuzman and Ayal Zaks, *Autovectorization in GCC – two years later*, GCC Developers' Summit 2006, June 28–30, Ottawa, Canada. pp. 145–158.
16. Mostafa Hagog and Ayal Zaks, *Swing Modulo Scheduling in GCC*, GCC Developers' Summit 2004, June 2–4, Ottawa, Canada. pp. 55–64.
17. Dorit Naishlos, Marina Biberstein and Ayal Zaks, *Compiler Vectorization Techniques for a Disjoint SIMD Architecture*, IBM Research Report H-0146, November 17, 2002. (Presented at a Compiler and Architecture seminar, IBM Haifa Lab, on Nov 25, 2002).
18. Marina Biberstein, Vugranam C. Sreedhar and Ayal Zaks *A Case for Sealing Classes in Java*, Israeli Workshop on Programming Languages & Development Environments, July 1, 2002.
19. Mayan Moudgill and Ayal Zaks, *Minimizing Inter-File Transfers in Architectures with Separate Address Registers*, IBM Research Report RC 21884 (98461), November 16, 2000.

Talks, Tutorials and more

- Invited to Dagstuhl Seminar 18111 on *Loop Optimization*, March 11–16, 2018, Dagstuhl, Germany.
- Co-organizing Compiler, Architecture and Tools event at Intel, Haifa, December 4, 2017. (software.intel.com/compilerconf2017)
- Gave an invited talk on *Extending LoopVectorizer towards supporting OpenMP4.5 SIMD and outer loop auto-vectorization* at an INRIA Seminar in Grenoble, France on December 14, 2016.
- Co-organizing Compiler, Architecture and Tools event at Intel, Haifa, November 23, 2015. (software.intel.com/compilerconf2015)
- Gave an invited talk on *Compiling for Scalable Computing Systems the Merit of SIMD* at The 5th Annual Henry Taub International TCE Conference in the Technion on June 2, 2015.
- Co-organizing Compiler, Architecture and Tools event at Intel, Haifa, December 1, 2014.
- Gave an invited talk on *Dynamic Compilation in OpenCL - Potential and Practice* at a Dynamic Compilation Day in Grenoble, France on November 12, 2014.

- Co-organizing Compiler, Architecture and Tools event at Intel, Haifa, November 18-19, 2013.
- Tutorial on *Optimizing with OpenCL on Intel Xeon Phi* with Arik Narkis, at the 2013 International Symposium on Code Generation and Optimization (CGO), February 24, 2013, Schenzen, China and at the 1st International Workshop on OpenCL (IWOCL), May 13-14, 2013, Atlanta, GA, USA.
- Organized thematic session on *Intermediate Representations* at HiPEAC Computing Systems Week, May 2-3, 2013, Paris, France.
- Co-organized Compiler, Architecture and Tools event at Intel, Haifa, November 26, 2012.
- Talk on Compilation guiding and adjusting to hardware changes in Embedded Reconfigurable Architecture (ERA) at the annual international event of the Israeli semiconductor industry (ChipEx), May 4, 2011, Tel-Aviv, Israel.
- Invited talk on *Driving Compiler Optimizations Efficiently*, June 24, 2010, Ghent University, Belgium.
- Panelist on *Compilers for embedded systems, a major industrial challenge* at ESWEEK 2009, October 11–16, Grenoble, France.
- Invited colloquium talk on *Driving Compiler Optimizations Efficiently*, September 21, 2009, at TU Delft, the Netherlands,.
- Co-organized StreamPPOT tutorial (on Embedded Streaming: Parallel Programming, Optimizations and Tools), June 12, 2009, co-located with ICS 2009, IBM T.J. Watson Research Center, Yorktown Heights, NY.
- Vice-chair for *High-performance architecture and compilers* topic, EuroPar'08.
- Invited to Dagstuhl Seminar 07361 on *Programming Models for Ubiquitous Parallelism*, September 2–7, 2007, Dagstuhl, Germany. Gave a talk on *Unleashing the power of simdization*.
- Technologies Magazine Embedded Conference, February 14, 2007, Tel-Aviv, Israel. Gave a talk on *GCC for Embedded Systems*.
- Co-organized GREPS workshop (GCC for Research in Embedded and Parallel Systems; later became GROW) with Albert Cohen, co-located with PACT 2007.
- Co-organized two HiPEAC GCC Tutorials in May 2006 (Grenoble, France) and January 28, 2007 (Ghent, Belgium).
- Co-editor of International Journal of Parallel Programming (IJPP) Special Issue, Vol 34, No.2, April 2006.

Patents

Coauthor of twenty issued patents on

- *Apparatus and Method for Updating Pointers for Indirect and Parallel Register Access* (7017028, 20040181646)
- *Apparatus for multiplication of data in two's complement and unsigned magnitude formats* (20040010536)
- *Creating Register Dependencies to Model Hazardous Memory Dependencies* (20100058034)
- *Digital signal processor with SIMD organization and flexible data manipulation* (20040015677)
- *Method and system for modeling non-interlocked diversely bypassed exposed pipeline processors for static scheduling* (20040123072)
- *Method for Identifying Sealed Calls in Java Packages* (6526571)
- *SIMD Processor with Concurrent Operation of Vector Pointer Datapath and Vector Computation Datapath* (6915411)
- *Software Pipelining Using One or More Vector Registers* (8136107, 20090113168)
- *Technique of Clustering and Compaction of Binary Trees* (6567815)
- *Transferring Data from Integer to Vector Registers* (7516299, 20100106939, 20070050598)
- *Vectorization in a SIMdD DSP Architecture* (7313788, 20050097301)
- *Management of conditional branches within a data parallel system* (20120198425)
- *Instance-based field affinity optimization* (20110239197)
- *Architecture-aware field affinity estimation* (20110302561)
- *On-line optimization of software instruction cache* (20110145503)
- *Vectorization of program code* (20110029962)
- *Monitoring Data Access Requests to Optimize Data Transfer* (20130013666)
- *Register Management in an Extended Processor Architecture* (20130138922)
- *Optional Branches* (20140189330)
- *Method and Apparatus for Cache Occupancy Determination and Instruction Scheduling* (20150089139)